POST-CORRELATION INTERPOLATION FOR DELAY LOCKED LOOPS

Abstract

A Code Division Multiple Access (CDMA) post-correlation processing system (12) for delay locked loop processing reduces the control data rate into a delay locked loop (DLL) processor and the number of required interpolation operations by executing a portion of the interpolation operations at a symbol data rate rather than at a chiprate. Specifically, an interpolator (16) generates time shifted chip samples based on input CDMA chip samples. First and second correlators (22, 24) extract ontime control and data symbol samples, respectively, from ontime input CDMA chip samples. A third correlator (26) extracts first non-ontime control symbol samples from non-ontime CDMA chip samples. The first non-ontime control symbol samples are then input with the ontime control symbol samples to a post-correlation interpolator (28) operating at a symbol rate to generate second non-ontime symbol samples necessary for Delay Locked Loop (DLL) processing.